AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-4. (Canceled without prejudice or disclaimer).

5. (New) A semiconductor integrated circuit comprising:

a first CPU accessing a first memory space with address translations and a second memory space without address translations;

an address translation circuit;

a nonvolatile memory to store address information indicating a relationship between an address of the first memory space and an address of the second memory space;

a first protocol decode and generation circuit connecting to a first bus connected to the first memory space; and

a second protocol decode and generation circuit connecting to a second bus connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register, and

an address calculation circuit,

wherein, when the semiconductor integrated circuit is initialized, the register reads the address information from the nonvolatile memory; and

wherein, when the semiconductor integrated circuit acts as a bus master to access the first memory space, the second protocol decode and generation circuit receives a first address in the second memory space and sends the first address to the address calculation circuit, the address calculation circuit translates the first address into a second address in the first memory space from the address information stored in the register, and the address calculation circuit sends the second address to the first protocol decode and generation circuit.

6. (New) The semiconductor integrated circuit according to claim 5, wherein the address information is stored in the nonvolatile memory when a probing test is conducted on the semiconductor integrated circuit.

7. (New) A semiconductor integrated circuit comprising:

a first CPU accessing a first memory space with address translations and a second memory space without address translations;

an address translation circuit;

a nonvolatile memory;

a first protocol decode and generation circuit connecting to a first bus connected to the first memory space; and

a second protocol decode and generation circuit connecting to a second bus connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register, and

an address calculation circuit,

wherein the nonvolatile memory stores a first start address in a first memory range belonging to the first memory space and a second start address in a second memory range belong to the second memory space;

wherein the second memory range is allocated to the first memory range;

wherein, when the semiconductor integrated circuit is initialized, the register reads the first start address and the second start address from the nonvolatile memory; and

wherein, when semiconductor integrated circuit acts as a bus master to access the first memory space, the second protocol decode and generation circuit receives a first address in the second memory range and sends the first address to the address calculation circuit, the address calculation circuit translates the first address into a second address in the first memory range from the first start memory address, the second start memory address, and the first address which are stored in the register, and the address calculation circuit sends the second address to the first protocol decode and generation circuit.

8. (New) The semiconductor integrated circuit according to claim 7:

wherein the address calculation circuit translates the first address into the second address from a formula: the first start address + the first address - the second start address.

9. (New) The semiconductor integrated circuit according to claim 7:

wherein the nonvolatile memory further stores a first address width of the first memory range;

wherein the address translation circuit further comprises an address selection circuit and an interrupt circuit;

wherein, when the semiconductor integrated circuit acts as a bus master to access the first memory space, the address selection circuit decides whether or not the first address belongs to the second memory range; and

wherein the address selection circuit sends an error signal to the address selection circuit if the first address doesn't belong to the second memory range.

10. (New) The semiconductor integrated circuit according to claim 7:

wherein the nonvolatile memory stores a third start address in a third memory range belonging to the second memory space and a fourth start address in a fourth memory address belonging to the first memory space;

wherein the fourth memory range is allocated to the third memory range;

wherein, when the semiconductor integrated circuit is initialized, the register reads the third start address and the fourth start address from the nonvolatile memory; and

wherein, when a second CPU acts as a bus master to access the second memory space, the first protocol decode and generation circuit receives a third address in the first memory range and sends the third address to the address calculation circuit, the address calculation circuit translates the third address into a fourth address in the fourth memory range from the third start memory address, the

fourth start address, and the third address which are stored in the register, and the address calculation circuit sends the fourth address to the second protocol decode and generation circuit.

11. (New) A semiconductor integrated circuit according to claim 5, wherein the address translation circuit is part of a flexible bus controller which is separate from the CPU.

12. (New) A semiconductor integrated circuit according to claim 7, wherein the address translation circuit is part of a flexible bus controller which is separate from the CPU.

13. (New) A semiconductor integrated circuit according to claim 11, wherein said flexible bus controller further comprises said first and second protocol decode and generation circuits.

14. (New) A semiconductor integrated circuit according to claim 12, wherein said flexible bus controller further comprises said first and second protocol decode and generation circuits.

15. (New) A semiconductor integrated circuit comprising:

a first CPU accessing a first memory space with address translations and the second memory space without address translations;

a peripheral LSI, separate from the first CPU, to transfer data between said first CPU and a peripheral device, said peripheral LSI comprising:

an address translation circuit;

a nonvolatile memory to store address information indicating a relationship between an address of the first memory space and an address of the second memory space;

a first protocol decode and generation circuit connecting to a first bus connected to the first memory space; and

a second protocol decode and generation circuit connecting to a second bus connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register, and

an address calculation circuit.

16. (New) A semiconductor integrated circuit according to claim 15, wherein the peripheral LSI further comprised a flexible bus controller which includes said address translation circuit and said first and second protocol decode and generation circuits.